POST-COMPENSATION OF A CT FIRST-ORDER ΣΔ ADC USING PWL DYNAMIC SYSTEMS

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***Abstract* — An approach for compensating nonlinearities in a continuous-time first-order sigma-delta converter with one bit quantization is presented. The proposed compensators are parallel nonlinear dynamic systems using piecewise linear static functions. A reduction of an order of magnitude is obtained in the measured squared error when compared to the uncompensated sigma-delta converter. Our results confirm a significant improvement in signal to noise and distortion ratio for single tone input signals and in spurious free dynamic range for multi-tone inputs.**

***Keywords*— Analog to digital converters, nonlinearities, PWL models, compensation.**

I. INTRODUCTION

Recently, the need for high resolution analog to digital converters (ADCs) with low power consumption, especially for mobile applications, has drawn much attention towards sigma-delta architectures for signal conversion. Such devices combine low resolution quantization with oversampling and noise shaping in order to reduce the in-band noise and thus increase the dynamic range. In particular, continuous-time (CT) sigma-delta modulators (SDMs) seem to be an attractive choice because of their inherent anti-aliasing properties and low circuit complexity, among other advantages (Van der Plassche, 2003). Sigma-delta structures have been proposed for many applications, including digital video broadcasting-terrestrial (DVB-T; see Ryan and Mahdi, 2009; Bonizzoni *et al.*, 2008; Jeong *et al.*, 2008) and Bluetooth (Yang *et al.*, 2009). In addition, they provide a flexible choice between resolution and bandwidth, which makes them suitable for multi-standard transceiver architectures combining for example GSM/WLAN/Bluetooth (Morgado *et al.*, 2006; Jose *et al.*, 2007).

Despite of the attractive properties, non-ideal circuit behavior degrades the overall performance resulting in harmonic distortion and increased in-band noise, which reduces the effective number of bits (ENOB) in the converter. A possible solution to reduce this distortion is to use model-based digital post-compensation techniques. These techniques generally consist on applying certain nonlinear dynamic function at the output of the converter such that the distortions originated by non ideal behavior of the device would be cancelled out (Vito *et al.*, 2007; Irons *et al.*, 1991). First, the post-compensator is trained (off-line) using measurement data from the CT SDM. Then, the identified compensator is implemented on-line during normal operation. This methodology involves some extra digital processing, i.e., a few multiplications and additions in the digital domain to obtain the corrected output sample.

In order to obtain an adequate structure for the compensator it is first necessary to understand the non-ideal behavior of CT SDMs. In Schmidt *et al.* (2011), it is shown that sigma-delta converters (SDCs) present weak nonlinearities and allow for a Volterra representation. Thus, they can be *p*-linearized with a Volterra system of similar complexity to that of the SDC model (Schetzen, 1980). In Schmidt *et al.* (2011), parallel polynomial dynamic systems belonging to the Volterra model family are proposed as compensators. Here, we explore the viability of piecewise linear (PWL) dynamic systems with efficient structure to keep the amount of parameters low. We show that the results in harmonic cancelation and signal to noise and distortion ratio (SINAD) improvement are good and also consistent with previous results.

The paper is organized as follows. In Section II models for a CT SDM are presented. The main contribution of this article, i.e. the proposed compensator is described in Section III. Section IV described the simulation results and the paper ends in Section V with some conclusions.

II. MODELS OF A CT SDM

A. Behavioral model

The general hypothesis behind a post-compensation strategy using a finite Volterra model considers that the SDM behavior is well described by a weakly nonlinear system.

We start from the ideal SDM shown in Fig. 1 consisting of three blocks (integrator, quantizer and digital to analog converter (DAC)) connected in a feedback loop. In Schmidt *et al.* (2011), we consider a model for each block introducing the real effects that preclude SDM ideal behavior, and we find an equivalent block oriented model, illustrated in Fig. 2, that represents the non-ideal SDM. In the diagram $P(\cdot)$ and $N(\cdot)$ represent weak static nonlinearities and $I(s)$ and $H(s)$ represent linear finite impulse response (FIR) dynamic blocks.

The integrator in the SDM, as discussed in Leuciuc (2001), can be replaced by a third order polynomial $P(\cdot)$ followed by an ideal integrator (i.e., a linear filter $I(s)$).