FPGA DESIGN OF AN EFFICIENT AND LOW-COST SMART PHONE INTERRUPT CONTROLLER

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***Abstract*— In this work we have designed and implemented an efficient platform-level interrupt controller for a PXA270 microprocessor-based smart phone. Although current hardware development boards include this type of controllers, for specific applications most of them are costly and include too many interrupt sources that represent a waste for a particular design. For this reason we designed our own interrupt controller which is capable of detecting interrupt sources coming from different devices that request microprocessor service. The developed interrupt controller is efficient and low-cost due to the small number of register and logic gates required for its implementation, as well as for the small number of levels to be traversed in the circuit´s critical execution path.**

***Keywords*— Interrupt controller, Codesign, FPGA, low-cost, effective, PXA270, smart phone.**

I. INTRODUCTION

Specific-purpose microprocessors are involved in the design of mobile digital systems, such as PDAs or Smart Phones. A microprocessor provides flexibility and scalability to the system. The flexibility is due to different programs being implemented with the same hardware. The scalability is due to the integration of additional hardware components by just modifying routines in the application program.

When the system performs several applications, the hardware and software become more complex. On the hardware side, additional devices are needed.

On the software side a manager program, like a real-time operating system is required, otherwise conflicts among different devices may arise. One effective mechanism to manage hardware devices is an interrupt controller.

An interrupt controller is a hardware component capable of detecting request signals coming from different devices. The request signals are generated by devices to indicate that they need some service to continue working. For example, pressing a keyboard key attached to a personal computer sends the equivalent digital code to the CPU. In there, an interrupt controller detects that the keyboard device needs attention, therefore an interrupt service routine is assisted in order to activate the input port associated to the keyboard and read it. The data that was read from the port corresponds to the value of the pressed key. Afterwards, depending on the application being used, for example a word processor, the available data might be displayed in the screen at the current cursor position.

In a more complex microprocessor-based architecture, which contains a high number of peripheral devices, it is desirable to have an interrupt controller to identify which device makes requests at which time. These devices must allow the microprocessor to define the priority level of each interrupt service.

In this work we developed a FPGA platform-level hardware software codesign of an efficient and low-cost interrupt controller for a smart phone to manage requests originated by several devices. The developed interrupt controller involved a hardware software codesign process because the smart phone is being designed for a particular operating system (Windows, 2005) and the interrupt controller features have taken into account the target operating system characteristics, to enhance the development and maintenance of the smart phone. The interrupt controller has been designed for a particular smart phone that is being designed as a cooperative effort between the authors´ institutions with the support of Instituto Tecnológico de Monterrey, Intel Corporation and the Secretaría de Economía de México, among others. The smart phone is to become a commercial product within this year. We have developed this interrupt controller because the available hardware development board of the used microprocessor needs and external interrupt controller in order to service I/O devices hierarchically.

In our design the core microprocessor is an Intel PXA270 (Intel, 2004a; Intel, 2004b; Intel, 2004c; Intel, 2004d; Intel, 2004e; Intel, 2004f; Intel, 2004g). Although the PXA270 has a hardware-level interrupt controller, a platform-level is needed. This type of controller allows handling requests from a device source to the appropriate target device. It also allows having several requests coming from the same device.

The rest of the paper is organized as follows. The Related Work section describes some previous interrupt controller designs. The Implementation of the Platform-level Interrupt Controller section explains our design in detail. The section Evaluation of the Interrupt Controller