## FORWARD AND INVERSE 2-D DCT ARCHITECTURES TARGETING HDTV FOR H.264/AVC VIDEO COMPRESSION STANDARD

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Abstract — This paper presents the architecture and the VHDL design of the integer Two-**Dimensional Discrete Cosine Transform (2-D DCT)** used in the H.264/AVC codecs. The forward and inverse 2-D DCT architectures were designed and their synthesis results mapped to Altera FPGAs are presented. The 2-D DCT calculation is performed by exploring the separability property, in such way, each 2-D DCT architecture is divided in two 1-D DCT calculations that are joined through a transpose buffer. The 1-D DCT transforms implemented and herein described are multiplierless, hence optimized shift-add operations are used. The architectures have a dedicated pipeline, optimized to process one input data per clock cycle. These architectures are able to cope with H.264/AVC encoder or decoder requirements targeting High Definition Digital Television (HDTV), with 1920x1080 pixel/frame at 30 frames per second.

*Keywords* — H.264/AVC video compression, dedicated hardware for video compression, 2-D FDCT, 2-D IDCT, integer transforms.

## I. INTRODUCTION

The H.264/AVC is the new international standard for video compression (Joint Video Team, 2003). The main characteristic of the H.264/AVC is to provide significantly higher compression rates than the previous standards as MPEG-2, MPEG-4 and H.263 (Wiegand *et al.*, 2003; Sullivan *et al.*, 2004; Sullivan and Wiegand, 2005). The H.264, also known as MPEG4 part 10 or AVC, was developed to supply the processing rates demanded by video applications in high definition.

An important factor that differentiates the H.264/AVC from other video compression standards is the use of integer transforms (Richardson, 2003; Malvar *et al.*, 2003). The integer transforms have a final result that is an approximation of the real transforms result. The H.264/AVC standard defines the use of two different integer transforms: 2-D DCT and Hadamard. These integer transforms are multiplierless and all

operations could be realized using just additions, subtractions and shift-adds.

Differently from other standards, the H.264/AVC defines a minimum image partition matrix (called block) with 4 x 4 samples. This option reduces the block and borders artifacts in the compressed image.

With the use of integer coefficients and 4x4 input blocks, the complexity of the transforms in the H.264/AVC is significantly reduced in relation to other image and video compression standards.

This paper will present the architectural design of a 2-D FDCT and a 2-D IDCT targeting the H.264/AVC compression standard. The 2-D DCT separability property was used in these architectures: the 2-D transforms are calculated by applying twice the transforms in one dimension which are joined by a transpose buffer. The designed architectures were described in VHDL (Airan *et al.*, 1994) and synthesized to Altera FPGAs (Altera, 2006). The synthesis results are also presented.

This paper is organized as follows. Section 2 presented an introduction to the H.264/AVC standard. Section 3 details the integer transform used in this standard. Section 4 presents the designed architectures. The synthesis results for the designed architectures are showed in section 5. Section 6 presets a comparison with related works. Conclusions and future works are presented in section 7.

## II. THE H.264/AVC STANDARD

An increasing number of services and the growing popularity of high definition TV are creating greater needs for higher coding efficiency. As a result of the ongoing demand for better compression performance the latest video coding standard, the H.264/AVC (Advanced Video Coding) (Joint Video Team, 2003) was developed. The H.264/AVC is also known as MPEG-4 Part 10 (Wiegand *et al.*, 2003; Sullivan *et al.*, 2004; Richardson, 2003).

H.264/AVC uses the state-of-the-art coding tools and provides enhanced coding efficiency for a wide range of applications (Wiegand *et al.*, 2003; Sullivan *et*